WHAT IS CLAIMED IS:

1. A method for scheduling a device command comprising:

issuing a first device command; and

issuing a first value, wherein the first value determines, at least in part, a first performance time at which the first device command is to be performed.

2. The method of claim 1, wherein the step of issuing a first device command comprises:

issuing a first memory device command and the first performance time is a time at which the first memory device command is to be performed.

3. The method of claim 2, wherein the step of issuing a first memory device command occurs at a first issuance time and the step of issuing a first value occurs at a second issuance time.

4. The method of claim 3, wherein the first issuance time and the second issuance time are different.

5. The method of claim 4, where the difference between the first issuance time and the second issuance time is a time gap.

6. The method of claim 5, wherein the time gap is predetermined.

7. The method of claim 5, wherein the time gap is fixed.

8. The method of claim 3, wherein the first value is a first delay value.

9. The method of claim 8, wherein the first delay value is expressed relative to a standardized unit of time.

10. The method of claim 8, wherein the first delay value is expressed in units of a clock period.

11. The method of claim 8, wherein the first delay value denotes an integer multiple of a clock period.

12. The method of claim 8, wherein the first delay value denotes a submultiple of a clock period.

13. The method of claim 8, wherein the first delay value has a positive or negative value.

14. The method of claim 13, wherein the first delay value has a value greater than zero.

15. The method of claim 13 wherein a delay between the first issuance time and the first performance time is determined by the first delay value and an additional delay value.

16. The method of claim 13, wherein a delay between the first issuance time and a first decoding time at which the first memory device command is decoded is determined by the first delay and an additional delay value.

17. The method of claim 13 wherein a delay between a first decoding time at which the first memory device command is decoded and the first performance time is determined by the first delay value and an additional delay value.

18. The method of claim 13, wherein the first issuance time and the second issuance time are the same.

19. The method of claim 13, wherein the first issuance time and the second issuance time are different, and the difference is a time gap.

20. The method of claim 19, wherein the time gap is predetermined.

21. The method of claim 20, wherein the first memory command is a column access strobe (CAS) command.

22. The method of claim 19, wherein the time gap is known at or before the first issuance time.

23. The method of claim 8 wherein the first memory device command is a precharge command.

24. The method of claim 8 wherein the first memory device command is a row access strobe (RAS) command.

25. The method of claim 8 wherein the first memory device command is a refresh command.

26. The method of claim 8 wherein the first memory device command comprises a refresh command and a row access strobe (RAS) command.

27. The method of claim 8 wherein the first memory device command comprises a refresh command and a pre-charge command.

28. The method of claim 8 wherein the first memory device command is a mode register operation command.

29. The method of claim 8 wherein the first memory device command is a power mode command.

30. The method of claim 8, wherein a first parameter associated with the first memory device

command is queued until the first performance time.

31. The method of claim 30 wherein the first parameter comprises a memory address.

32. The method of claim 31 wherein the first parameter comprises data to be stored in the first memory device.

33. The method of claim 2 wherein the first value is communicated from a memory controller to a first memory device.

34. The method of claim 1, further comprising:

issuing a second device command; and

issuing a second value, wherein the second value determines, at least in part, a second performance time at which the second device command is to be performed.

35. The method of claim 34, wherein the step of issuing a first device command comprises issuing a first memory device command, the step of issuing a second device command comprises issuing a second memory device command, the first performance time is a first time at which the first memory device command is to be performed, and the second performance time is a second time at which the second memory device command is to be performed.

36. The method of claim 35, wherein the step of issuing the first memory device command occurs at a first issuance time, the step of issuing the first value occurs at a second issuance time, the step of issuing the second memory device command occurs at a third issuance time, and the step of issuing the second value occurs at a forth issuance time.

37. The method of claim 36, wherein the first issuance time is the same as the second issuance time; and the third issuance time is the same as the fourth issuance time.

38. The method of claim 37, wherein the first issuance time and the third issuance time are different.

39. The method of claim 38, wherein a first difference between the first issuance time and the second issuance time is of equal duration to a second difference between the third issuance time and the fourth issuance time.

40. The method of claim 39 wherein the first difference is known at or before the first issuance time.

41. The method of claim 38, wherein the first value is a first delay value and the second value is a second delay value.

42. The method of claim 41, wherein the second delay value is different than the first delay value.

43. The method of claim 35, wherein the second delay value is the same as the first delay value.

44. The method of claim 35, wherein the first performance time is after the second performance time.

45. The method of claim 3, wherein the first value is a first index value.

46. The method of claim 45, wherein a first parameter associated with the first memory device command is queued until the first performance time.

47. The method of claim 45 wherein the first memory device command is a precharge command.

48. The method of claim 45 wherein the first memory device command is a row access strobe (RAS) command.

49. The method of claim 45 wherein the first memory device command is a refresh command.

50. The method of claim 45 wherein the first memory device command comprise a refresh command and a row access strobe (RAS) command.

51. The method of claim 45 wherein the first memory device command comprise a refresh command and a pre-charge command.

52. The method of claim 45 wherein the first memory device command is a mode register operation command.

53. The method of claim 45 wherein the first memory device command is a power mode command.

54. The method of claim 45, further comprising the steps of determining a first delay value based on the first index.

55. The method of claim of claim 54, further comprising:

providing a look-up table having a plurality of delay values and associated addresses, wherein each of the delay values is associated with one of the addresses, wherein the first index value represents one of the addresses in the look-up table, and wherein the step of determining the first delay value comprises selecting the delay value associated with the address of the first index.

56. The method of claim 34, wherein the first value is a first index value and the second value is a second index value.

57. The method of claim 56, further comprising the steps of
determining a first delay value based on the first index; and
determining a second delay value based on the second index.

58. The method of claim of claim 57, further comprising:
providing a look-up table having a plurality of delay values and associated addresses, wherein each of the delay values is associated with one of the addresses, wherein the first index represents a first addresses in the look-up table, wherein the step of determining the first delay value comprises selecting the delay value associated with first address, wherein the second index represents a second address in the look-up table, and wherein the step of determining the second delay value comprises selecting the delay value associated with second address.

59. The method of claim 58, wherein the first and second address are the same address.

60. The method of claim 59, wherein the first and second addresses are different addresses.

61. The method of claim 58, wherein the step of providing a look-up table comprises the steps of providing a first look-up table and a second look-up table, and wherein the first address is associated with the first look-up table and the second address is associated with the second look-up table.

62. The method of claim 57, wherein the first delay value determines, at least in part, a first performance time at which the first device command is to be performed, and wherein the second delay value determines, at least in part, a second performance time at which the second device command is to be performed.

63. The method of claim 34 wherein the first device command is sent to a first memory device at a first issuance time, and the second device command is sent to a second memory device at a second issuance time, the first issuance time being different from the second issuance time, wherein the first device command is performed at the first memory device while the second device command is performed at the second memory device.

64. A controller for scheduling commands comprising:

a driver for issuing commands and associated non-zero delay values to at least one device coupled to the controller, wherein a first delay value is associated with a first performance time at which a first command of the commands is to be performed by the device.

65. The controller of claim 64, wherein the driver comprises:

a first driver for issuing commands to the device and a second driver for issuing delay values to the device.

66. The controller of claim 64 wherein the controller is a memory controller.

67. The controller of claim 66 wherein the device is a memory device.

68. The controller of claim 64 wherein the driver issues the first command with a first delay value for performance of the first command at the first performance time and a second command with a second delay value for performance of the second command at a second performance time.

69. The controller of claim 64 wherein the controller determines performance constraints of the device to determine the first performance time and the second performance time.

70. The controller of claim 69 wherein the performance constraints are dependent upon a physical location of the device relative to the controller.

71. The controller of claim 69 wherein the performance constraints are dependent upon a

propagation delay affecting reception of the first command at the device.

72. The controller of claim 69 wherein the performance constraints are dependent upon a propagation delay affecting reception of the data from the device.

73. The controller of claim 69 wherein the performance constraints are dependent upon a state of the device.

74. The controller of claim 69 wherein the performance constraints are dependent upon an operational speed limitation of the device.

75. The controller of claim 69 wherein the performance constraints are dependent upon a difference in timing granularity between an internal bus of the device and an external bus coupling the device to the controller.

76. The controller of claim 64 wherein the controller issues the first command at a first issuance time.

77. The controller of claim 76 wherein a delay between the first issuance time and the first performance time is determined by the first delay value and an additional value.

78. The controller of claim 76 wherein a delay between the first issuance time and a first decoding time at which the first command is decoded is determined by the first delay value and an additional delay value.

79. A device comprising:

a receiver for receiving a first device command, a first value associated with the first device command, wherein a first performance time is associated with the first value;

means for performing the first device command at the first performance time; and

control circuitry for controlling the means to cause the means to perform the first device command at the first performance time.

80. The device of claim 79 wherein the receiver is also for receiving a second device command and a second value associated with the second device command.

81. The device of claim 80 wherein a second performance time is associated with the second value.

82. The device of claim 81 wherein the means is also for performing the second device command at the second performance time.

83. The device of claim 80 wherein the second value is different from the first value.

84. The device of claim 80 wherein the second value is a delay value.

85. The device of claim 80 wherein the second value is an index value.

86. The device of claim 79 wherein the first value is a first delay value.

87. The device of claim 79 wherein the first value is a first index value.

88. The device of claim 79, wherein the first device command is a first memory device command, and the second device command is a second memory device command.

89. The device of claim 88, wherein the receiver comprises:
a first receiver for receiving the first device command; and
a second receiver for receiving the second device command.

90. The device of claim 89, wherein the first receiver is also for receiving the first index and the second receiver is also for receiving the second index.

91. The device of claim 89, wherein the first and second receivers are configured to receive the first and second device commands and the first and second indices from a controller.

92. The device of claim 91, wherein the controller is a memory controller.

93. The device of claim 88 wherein the first memory device command is a precharge command.

94. The device of claim 88 wherein the first memory device command is a row access strobe (RAS) command.

95. The device of claim 88 wherein the first memory device command is a refresh command.

96. The device of claim 88 wherein the first memory device command comprise a refresh command and a row access strobe (RAS) command.

97. The device of claim 88 wherein the first memory device command comprise a refresh command and a pre-charge command.

98. The device of claim 88 wherein the first memory device command is a mode register operation command.

99. The device of claim 88 wherein the first memory device command is a power mode command.

100. The device of claim 79 wherein the receiver first receives the first command and the first delay value, then later receives the second command and the second delay value, wherein the device performs the second command before performing the first command.

101. A system comprising

a first device configured to issue commands and values, wherein each of the values is associated with a respective one of the commands; and

a second device configured to receive the commands and the associated values; the second device further configured to execute each command at a time determined at least in part by the value associated with the command,

wherein the first device is further configured to dynamically determine the value associated with at least one of the commands.

102. The system of claim 1, wherein the first device is a memory controller and the second device is a memory device.

103. The system of claim 1, wherein each value is a delay value.

104. The system of claim 1, wherein each value is an index value which is representative of a delay value.

105. A system comprising:

a first device comprising

means for issuing commands; and

means for issuing values, wherein each of the values is associated with a respective one of the commands; and

a second device comprising:

means for receiving commands;

means for receiving the associated values; and

means for performing each of said commands at a time determined at least in part by the associated value.

106. The system of claim 1, wherein each value is a delay value.

107. The system of claim 1, wherein each value is an index value which is representative of a delay value.